Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A semiconductor memory, comprising:

a plurality of memory cells forming at least one memory cell array, the memory cells being connected to first lines and to second lines, the second lines crossing the first lines, each memory cell having a storage capacitor and a selection transistor, ~~the memory cells form at least one memory cell array,~~ wherein the first lines run divergently with respect to one another, the second lines are curved, a memory cell is connected at each crossing point between a first line and a second line, each of the first lines ~~having~~ has memory cells connected thereon, and [[the]] respective storage capacitors [[being]] are laterally offset alternately on each side of the respective first lines.

2. (Original) The semiconductor memory as claimed in claim 1, wherein the first lines extend divergently from a logic area to the memory cells in at least one memory cell array.

3. (Currently Amended) The semiconductor memory as claimed in claim 1, wherein the ~~memory cells form~~ at least one memory cell array~~, at the memory cell array having the form of~~ forms an annular portion, the first lines diverging radially, and the second lines curving arcuately.

4. (Original) The semiconductor memory as claimed in claim 1, wherein one or more memory cell arrays surround a logic area annularly.

5. (Original) The semiconductor memory as claimed in claim 1, wherein the first lines are bit lines and the second lines are word lines.

6. (Original) The semiconductor memory as claimed in claim 1, wherein the first lines are word lines and the second lines are bit lines.

7. (Currently Amended) The semiconductor memory as claimed in claim 1, wherein one of the first and second lines are bit lines and the other of the first and second lines are word lines and two memory cells are connected to two mutually adjacent bit lines~~, the two memory cells being connected to~~ and to the same word line, the two memory cells having respective storage capacitors adjacent to one another along the same word line~~, the two memory cells being connected to two mutually adjacent bit lines~~.

8. (Original) The semiconductor memory as claimed in claim 1, wherein the storage capacitors are trench capacitors buried in a semiconductor substrate.

9. (Currently Amended) The semiconductor memory as claimed in ~~claim 8~~ claim 4, wherein at least one further logic area is provided on [[the]] a semiconductor substrate and is arranged between a memory area and an edge of the semiconductor substrate, the further logic area not being surrounded by memory areas.

10. (Currently Amended) The semiconductor memory as claimed in claim 1, wherein the first lines or the second lines are word lines and the selection transistors are vertical field effect transistors whose gate electrodes are connected to the word lines.

11. (Canceled)

12. (Original) The semiconductor memory as claimed in claim 1, wherein the semiconductor memory is a dynamic read/write memory.

13. (Currently Amended) A semiconductor memory, comprising:

a plurality of memory cells forming at least one memory cell array, the memory cells being connected to first lines and to second lines, the second lines crossing the first lines, each memory cell having a storage capacitor and a selection transistor, ~~the memory cells form at least one memory cell array,~~ wherein the first lines run divergently with respect to one another, the second lines are curved, a memory cell is connected at each crossing point between a first line and a second line, each of the second lines ~~having~~ has memory cells ~~being~~ connected thereon, and [[the]] respective storage capacitors [[being]] are laterally offset alternately on each side of the respective second lines.

14. (Original) The semiconductor memory as claimed in claim 13, wherein the first lines extend divergently from a logic area to the memory cells in at least one memory cell array.

15. (Currently Amended) The semiconductor memory as claimed in claim 13, wherein the ~~memory cells form~~ at least one memory cell array~~, the memory cell array having the form of~~ forms an annular portion, the first lines diverging radially, and the second lines curving arcuately.

16. (Original) The semiconductor memory as claimed in claim 13, wherein one or more memory cell arrays surround a logic area annularly.

17. (Original) The semiconductor memory as claimed in claim 13, wherein the first lines are bit lines and the second lines are word lines.

18. (Original) The semiconductor memory as claimed in claim 13, wherein the first lines are word lines and the second lines are bit lines.

19. (Currently Amended) The semiconductor memory as claimed in claim 13, wherein one of the first and second lines are bit lines and the other of the first and second lines are word

lines and two memory cells are connected to two mutually adjacent bit lines~~, the two memory cells being connected to~~ and to the same word line, the two memory cells having respective storage capacitors adjacent to one another along the same word line~~, the two memory cells being connected to two mutually adjacent bit lines~~.

20. (Original) The semiconductor memory as claimed in claim 13, wherein the storage capacitors are trench capacitors buried in a semiconductor substrate.

21. (Currently Amended) The semiconductor memory as claimed in ~~claim 20~~ claim 16, wherein at least one further logic area is provided on [[the]] a semiconductor substrate and is arranged between a memory area and an edge of the semiconductor substrate, the further logic area not being surrounded by memory areas.

22. (Currently Amended) The semiconductor memory as claimed in claim 13, wherein the first lines or the second lines are word lines and the selection transistors are vertical field effect transistors whose gate electrodes are connected to the word lines.

23. (Canceled)

24. (Currently Amended) The semiconductor memory as claimed in ~~claim 12~~ claim 13, wherein the semiconductor memory is a dynamic read/write memory.

25. (New) The semiconductor memory as claimed in claim 1, wherein the first lines run divergently in non-parallel directions along their extent.

26. (New) The semiconductor memory as claimed in claim 1, wherein the first lines are continuously divergent along their extent.

27. (New) The semiconductor memory as claimed in claim 1, wherein the second lines extend along concentric arcs.

28. (New) The semiconductor memory as claimed in claim 13, wherein the first lines run divergently in non-parallel directions along their extent.

29. (New) The semiconductor memory as claimed in claim 13, wherein the first lines are continuously divergent along their extent.

30. (New) The semiconductor memory as claimed in claim 13, wherein the second lines extend along concentric arcs.

31. (New) A semiconductor memory, comprising:

a centrally-located logic area for operating the semiconductor memory;

at least one memory array surrounding the logic area;

first lines extending outward from the logic area into the at least one memory array;

second lines extending through the at least one memory array along a periphery of the logic area and arranged concentrically with respect to the logic area such that the first and second lines form a non-rectangular array of crossing points; and

a plurality of memory cells coupled to the first and second lines at the crossing points, the memory cells including storage capacitors laterally offset alternately on each side of respective first lines or respective second lines.